Non-Contact Interface

Noriyuki Miura
Keio University
Outline

► Introduction
  – 3D Non-Contact Interface (NCI)
  – Why 3D?
  – Why Non-Contact?

► NCI for 3D Chip Stacking
► NCI for 3D Module Connector
► NCI for Emerging Application
► Summary
Non-Contact Interface

▶ For 3D-integrated chips and modules

Inter-Chip Interface: ThruChip Interface (TCI)
μm-distance, >1Tb/s

Inter-Module Interface: Coupled Transmission Lines (CTL)
mm-distance, >10Gb/s

Main Processor Module

Sub Module

Main Board

NAND

DRAM

Processor

Inductive Coupling

Electro-Magnetic Coupling

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Why 3D?

- Exponentially-increasing integration demand

![Graph showing memory capacity and technology node over time. The graph illustrates the trend in memory capacity from 1994 to 2024, with markers for Mass Storage, NAND Chip, MLC, 3D Chip Stacking, and 2D Scaling Limit. The graph indicates exponential growth in memory capacity with a technology node that scales at 1.5x/Year for MLC, 2x/Year for NAND Chip, and 2x/Year for Mass Storage.](image-url)
Why 3D? (2)

► Rapid growth in bandwidth requirement

![Graph showing the growth of memory bandwidth over years with different gaming consoles and graphics cards marked on the graph.](image)
Why 3D? (3)

Computation-to-communication performance gap

Computation: $1.15 \times 1.49 = 1.71x$

Area $\propto$ Computation

Communication $\propto$ Periphery

Communication: $1.15 \times 1.11 = 1.28x$

Periphery

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Why Non-Contact?

► Low cost
  – No additional process steps needed
  – Reduction in # of bonding wires or connectors

► Small size (small form factor)
  – Assembly complexity relaxed

► High performance
  – Interface antenna covered by protection layer
  – No ESD protection devices needed
  – Channel characteristics improved
Why Non-Contact? (2)

► User convenience
  – Relaxed alignment accuracy
  – Easily detachable

► Mechanical reliability
  – Long connector life span

► Potentials to open up emerging applications
Outline

► Introduction

► NCI for 3D Chip Stacking
  – ThruChip Interface (TCI)

► NCI for 3D Module Connector

► NCI for Emerging Application

► Summary
ThruChip Interface (TCI)

- Inductive coupling
- Digital CMOS circuit

- Coils by multi-layer wires
  - Logic interconnections can go through coil
  - Coils can be placed anywhere

65nm CMOS
TCI vs. TSV

Inexpensive yet competitive performance

Low-End | Applications | High-End
---|---|---
Automotive Digital Consumer | Cellular Phone PC, Storage Multimedia | Super Computer Server Game, Graphics

Wire Bonding

ThruChip Interface (TCI)

>20¢/chip Cost Down

High Power Delivery

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TCI vs. Wireless Transceivers

TCI utilizes near-field inductive coupling
Near Field vs. Far Magnetic

► Near field (TCI): small crosstalk, small ch. pitch

► Far field (WLAN): need crosstalk countermeasure
Channel Characteristics

► Ideal: 1\textsuperscript{st}-order differentiator (gain: $M$)

► Actual: Band pass filter (peak @ $f_{SR}$)

► Max. data rate < $f_{SR}/2$

\[ V_R = M \frac{dI_T}{dt} \times \text{Low Pass} \]

\[ \text{Ideal} \]

\[ \text{Parasitic} \]

$f_{SR}$: Self-Resonant Frequency

[1] N. Miura (VLSI’04)
TCI Transceiver Circuit

- Tx: H-bridge driver, Rx: Hysteresis comparator

Threshold Voltage
Communication Range

Typical communication range < 1/3 diameter

![Diagram showing the normalized coupling gain as a function of \(X/D\) with slopes \((X/D)^{-1}\) and \((X/D)^{-3}\). The graph illustrates the relationship between the normalized coupling gain and the distance ratio \(X/D\), with specific values for the communication range highlighted.](image)
Channel Pitch

▶ Line: 1~2x diameter, Array: 2~3x diameter

- Normalized Horizontal Distance $Y/D$
- Normalized Channel Pitch $P/D$

Crosstalk / Signal [dB]

$1/Y^2$ Slope

Array

$P_{Array} = 2D~3D$

Line

$P_{Line} = D~2D$

3D Scaling Scenario

► MOS transistor (2D scaling)

- Voltage: 1/2
- Size: 1/2
- Speed: 2x
- Power/Area: 1

Constant Electric Field Scaling

► TCI (3D scaling)

- Diameter: 1/2
- Thickness: 1/2
- Data Rate/Area: 8x
- Energy/bit: 1/8

Constant Magnetic Field Scaling

TCI Performance and Cost Significantly Improved by 3D Scaling

Silicon Proof

High Speed

1.2Gb/s/ch\textsuperscript{[4]} (ISSCC’04)
11Gb/s/ch\textsuperscript{[2]} (ISSCC’08)
30Gb/s/ch\textsuperscript{[5]} (ASSCC’10)

Low Power

140fJ/b\textsuperscript{[6]} (ISSCC’07)
65fJ/b\textsuperscript{[7]} (ASSCC’08)
10fJ/b\textsuperscript{[8]} (VLSI’10)

Wide Bandwidth

0.2Tb/s\textsuperscript{[9]} (ISSCC’05)
1Tb/s\textsuperscript{[10]} (ISSCC’06)
8Tb/s\textsuperscript{[11]} (ISSCC’10)

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Step Toward Practical Use

ISSCC’07
Bus Probe

ISSCC’09
SSD

ISSCC’09
MPU+SRAM

ISSCC’09
Non-Contact Wafer Test

VLSI’09
Cubic Processor

ISSCC’09
Non-Contact Wafer Test

ISSCC’09
SSD

ISSCC’10
Interposer

ISSCC’10
SSD

ISSCC’10
DRAM+GPU

ISSCC’11
SSD

ISSCC’11
Wafer Test

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► Introduction

► NCI for 3D Chip Stacking
   – TCI Application I: NAND Flash Memory Stacking

► NCI for 3D Module Connector

► NCI for Emerging Application

► Summary
NAND Flash Memory Stacking

Conventional SSD
x8 NAND Packages

Controller

16 NAND Chips

1/6

3,500 Wires in Total

580 Wires in Total

128 NAND Chip Stack

Inductive Coupling

Controller

Power Only

Read

Write

TCI

30 Wires/Chip

346 Wires in Total

198 Wires

1/6

One-Package SSD

[5] Y. Sugimori (ISSCC’09)

N. Miura (22/51)
128-Die NAND Stacking

64Gb x 128-Die = 8Tb = 1TB

IO Energy: 0.9pJ/b/chip @ 2.4Gb/s (1/15 of Conventional)

Relay Through Memory Chips

Relay at Every Chips

Relay at Every 8th Chips

1/8 Repeaters

Sleep

Measurement Setup

Average Number of Repeaters vs. Number of Chip Penetration, \( N_P \)

Total Tx Power vs. Tx Power/Repeater

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Coupled-Resonant Clock Link

Conventional

Proposed

Relay by TCI Repeater

Coupled Resonation

High Gain at Resonance

Clock Coil

Data Coil

Frequency

Power: 1/10

# Performance Comparison

## 128 NAND Flash Chips + 1 Controller Chip Stacking

<table>
<thead>
<tr>
<th></th>
<th>TCI</th>
<th>Wire Bonding</th>
</tr>
</thead>
<tbody>
<tr>
<td># of Bonding Wires in Package</td>
<td>546 (1/6)</td>
<td>3,409 (1)</td>
</tr>
<tr>
<td>Transmission</td>
<td>Transmission Relayed at Every 8(^{th}) Chip</td>
<td>Broadcast by Wired-OR of 64 Chips</td>
</tr>
<tr>
<td>Aggregated Data Rate</td>
<td>19.2Gb/s (30x)</td>
<td>0.64Gb/s (1)</td>
</tr>
<tr>
<td>IO Energy Consumption / Chip</td>
<td>0.9pJ/b (1/15)</td>
<td>13.6pJ/b (1)</td>
</tr>
</tbody>
</table>

![Diagram of resonator with dimensions](image)


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► NCI for 3D Chip Stacking
  – TCI Application II: Processor-Memory Stacking

► NCI for 3D Module Connector

► NCI for Emerging Application

► Summary
Memory-Processor Stacking

SRAM Chip (65nm CMOS)
50μm-Thick, $V_{DD}=1.2$V
Stacked Face-up on Processor

Processor Chip (90nm CMOS)
50μm-Thick, $V_{DD}=1$V
Mounted Face-down on C4 Bump

[8] K. Niitsu (ISSCC’09)

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Technical Challenges

► Different design
► Different supply voltage
► Different process

1MB SRAM

Processor, $V_{DD}=1V$, 90nm CMOS

1MB SRAM, $V_{DD}=1.2V$, 65nm CMOS
Inductive-Coupling Interposer

Coils at different locations connected wirelessly

[9] S. Kawai (VLSI’09)
AC-Coupled Interface

► No need for level shifter
► No need for different $V_{DD}$, thick-oxide tr.

Quad Data Rate Architecture

Four-phase $1/4f$ clock used for MUX/DMUX

[10] N. Miura (ISSCC’10)
8Tb/s DRAM-GPU Interface

20mm-Thick 100nm DRAM Chip (Upper Chip)

1024ch Link Array

60μm

60μm

TCI in DRAM (Upper Chip)

TCI in GPU (Lower Chip)

65nm CMOS GPU Chip (Lower Chip)

[10] N. Miura (ISSCC’10)
### Performance Comparison

<table>
<thead>
<tr>
<th></th>
<th>TCI</th>
<th>*Wired XDR™</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bandwidth</strong></td>
<td>8Tb/s (x32)</td>
<td>0.25Tb/s (1)</td>
</tr>
<tr>
<td><strong>Data Rate</strong></td>
<td>8Gb/s/Link</td>
<td>16Gb/s/Link</td>
</tr>
<tr>
<td><strong>Number of Links</strong></td>
<td>1024</td>
<td>16</td>
</tr>
<tr>
<td><strong>Layout Area</strong></td>
<td>6.5mm²</td>
<td>4.4mm²</td>
</tr>
<tr>
<td><strong>Area / Bandwidth</strong></td>
<td>0.8mm²/Tb/s (1/22)</td>
<td>17.2mm²/Tb/s (1)</td>
</tr>
<tr>
<td><strong>Power Dissipation</strong></td>
<td>8W</td>
<td>2W</td>
</tr>
<tr>
<td><strong>Energy / bit</strong></td>
<td>1pJ/b (1/8)</td>
<td>8pJ/b (1)</td>
</tr>
<tr>
<td><strong>BER</strong></td>
<td>&lt;10⁻¹⁶</td>
<td>&lt;10⁻¹⁵</td>
</tr>
<tr>
<td><strong>Process</strong></td>
<td>65nm CMOS &amp; Emulated 100nm DRAM</td>
<td>Emulated 40nm DRAM</td>
</tr>
</tbody>
</table>

*Rambus Inc. (VLSI’08)*
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► Introduction
► NCI for 3D Chip Stacking
► NCI for 3D Module Connector
  – Coupled Transmission Lines (CTL)
► NCI for Emerging Application
► Summary
Coupled Transmission Lines

- Electrical coupling and magnetic coupling

- Impedance-matched therefore wideband

Equivalent Circuit Model

Distributed LC Element Model

Frequency

Gain

CTL

Inductive Coupling

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Channel Design

- Length $L$ determines center operating $f$
- Space $S$, Width $W$ adjust characteristic $Z$
- Distance $d$ determines flat coupling gain

CTL Layout Parameters

<table>
<thead>
<tr>
<th>Coupling Gain [dB]</th>
<th>Frequency [GHz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>$d=1.0\text{mm}$</td>
<td>0</td>
</tr>
<tr>
<td>$L=4\text{mm}$</td>
<td>-10</td>
</tr>
<tr>
<td>$L=6\text{mm}$</td>
<td>-20</td>
</tr>
<tr>
<td>$L=10\text{mm}$</td>
<td>-30</td>
</tr>
</tbody>
</table>

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Robustness to Misalignment

-4.4dB @ +50% Distance
-1.7dB @ 0.5mm Offset

Coupling Gain [dB]
Frequency [GHz]
Distance $d$
Length $L$
Space $S$
Width $W$
CTL Transceiver Circuit

- Similar to TCI transceiver
- 50Ω Termination at each port

12Gb/s CTL Interface CTL

Communication performance
- 12Gb/s communication over 1mm distance
- BER<10^{-13}, timing margin>50% U.I.
Outline

► Introduction
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  – Non-Contact Memory Card
  – Permanent Memory: Digital Rosetta Stone
► Summary
Emerging Application

► Non-contact memory card
  - Both power and data delivered wirelessly
  - No mechanical contact → High reliability
  - No ESD protection → High-speed access

► Technical challenges
  - Power link:
    High power/efficiency
  - Data link:
    Immunity to interference from power link
Isolation between Data/Power Links

Strong interference from power link to data link
- 60dB (1,000x) too large input power in power link
- 80dB (10,000x) link isolation needed
- 40dB (100x) freq. difference not enough for filtering
Time Interleaving

Time Interleaving works but lowers data rate

![Diagram of power and data signals]

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**Differential Coil**

Power Link Coils

Data Link

Differential Coils

Data Transmission

Power Interference Cancel

[12] Y. Yuan (VLSI’10)
Simultaneous P/D Delivery

Data Rate 6Gb/s (>20x of Conventional Memory Card)
Bit Error Rate <10^{-14} (Comparable with Wired Interface)

[12] Y. Yuan (VLSI’10)
Digital Archive

► To archive digitalized cultural heritage (literature, art, or movie) for our descendant

► World Digital Library Project (UNESCO)
  – Cultural heritage 8000 BC – 2010 AD

► Digital Cinema Initiatives (Hollywood Studios)
  – Storing and maintaining high-resolution digital master cost around $12,500 per year

► Permanent (>1,000 year) memory required
Digital Rosetta Stone

Power/Data Link

Reader

Non-Contact

Power

[13] Y. Yuan (VLSI’09)

N. Miura (48/51)
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Summary

► 3D LSI integration
  – To meet rapid growth in performance requirement

► Non-contact interface (NCI)
  – Low-cost/high-performance/high-reliable link

► Inter-chip ThruChip Interface (TCI)
  – Inexpensive yet competitive performance to TSV
  – Cost/performance significantly improved by 3D scaling
  – Applicable to NAND stacking
  – Applicable to processor-memory stacking

► Inter-module Coupled Transmission Lines (CTL)
  – Wideband/long-distance communication between modules

► Non-contact power/data transfer
  – Opens up emerging 3D memory applications
  – Non-contact memory card, permanent memory system

► NCI matured enough for practical use